#### REMARKS

## Claim Rejections - 35 U.S.C. §102

The Examiner has rejected claim 11 under 35 U.S.C. 102(e) as being anticipated by <a href="Modes et al.">Cheung et al.</a> (U.S. Patent No.: 6,287,990). The Applicant respectfully traverses. <a href="Cheung does">Cheung does</a> not anticipate the Applicant's invention because <a href="Cheung does">Cheung does</a> not teach all elements of claim 11. <a href="Claim 11">Claim 11</a> is as follows:

- 11. A substrate processing system comprising:
  - a housing defining a process chamber;
- a substrate holder, located within said process chamber, for holding a silicon substrate which includes a silicon trench formed between upper portions and having a trench bottom and a trench wall;
  - a gas delivery system for introducing process gases into said process chamber; a controller for controlling said gas delivery system; and
- a memory coupled to said controller comprising a computer-readable medium having a computer-readable program embodied therein for directing operation of said controller, said computer-readable program including a set of instructions to control said gas delivery system to introduce a process gas including ozone and a precursor into said process chamber to form a dielectric layer on said silicon substrate, said precursor providing deposition rate dependence of said dielectric layer on differently constituted surfaces at different levels comprising said trench bottom and a material on said upper portions of said silicon substrate, and to adjust an ozone/precursor ratio between said ozone and said precursor until said dielectric layer develops a substantially planar dielectric surface.

<u>Cheung</u> does not teach the last highlighted element of claim 11. Specifically, <u>Cheung</u> does not teach a computer-readable program including instructions to control process gases including ozone and a precursor to form a dielectric layer where the precursor provides a deposition rate dependence on differently constituted surfaces and where the computer readable program includes instructions to adjust an ozone/precursor ratio between said ozone and said precursor until said dielectric layer develops a substantially planar dielectric surface. Therefore, <u>Cheung</u> does not anticipate claim 11.

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## Claim Rejections – 35 U.S.C. §103

The Examiner has rejected claims 1-10 and 16-27 under 35 U.S.C. 103(a) as being unpatentable over <u>Tsai et al.</u> (U.S. Patent No.: 5,930,644) in view of <u>Oh</u> (U.S. Patent No.: 6,372,606). The Applicant respectfully traverses. The elements of claims 1-10 and claims 16-27 are not all taught by <u>Tsai</u> in view of <u>Oh</u>. Claim 1 is as follows:

# 1. A method comprising:

providing a silicon substrate in a substrate processing chamber, said silicon substrate having upper portions;

forming a trench in said silicon substrate between said upper portions, said trench having a trench bottom and a trench wall;

introducing a precursor, preferably TEOS, into said substrate processing chamber to form a dielectric layer over said silicon substrate, the precursor providing a deposition rate dependence of said dielectric layer on differently constituted surfaces at different levels on said substrate, said differently constituted surfaces at different levels comprising said trench bottom and a material on said upper portions;

flowing ozone into said substrate processing chamber to react with said precursor to deposit a dielectric layer over said substrate; and

adjusting an ozone/precursor ratio between said ozone and said precursor to regulate deposition rates of said dielectric layer on said differently constituted surfaces until said dielectric layer develops a substantially planar dielectric surface.

Neither <u>Tsai</u> nor <u>Oh</u> teach the element in claim 1 of "adjusting an ozone/precursor ratio between said ozone and said precursor to regulate deposition rates of said dielectric layer on said differently constituted surfaces until said dielectric layer develops a substantially planar dielectric surface." An ozone/precursor ratio to regulate the deposition rate of a dielectric layer and to regulate the formation of a substantially planar dielectric surface are not discussed in either <u>Tsai</u> or <u>Oh</u>. Claims 2-10 are dependent on claim 1 and hence incorporate all limitations of claim 1. Therefore, claims 1-10 are not obvious in light of <u>Tsai</u> in view of <u>Oh</u>.

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#### Claim 16 is as follows:

16. A method for forming a trench isolation structure on a silicon substrate, the method comprising the steps of:

applying a CVD anti-reflective coating on and contacting said silicon substrate; forming a photoresist on said CVD anti-reflective coating;

exposing a portion of said photoresist to a light to define a location where a trench is to be formed;

removing said photoresist at said location; and

etching, at said location, through said CVD anti-reflective coating and through a depth of said substrate to form said trench at said location.

Neither <u>Tsai</u> nor <u>Oh</u> teach the element in claim 16 of "applying a CVD anti-reflective coating on and contacting said silicon substrate." In contrast, <u>Tsai</u> teaches forming an anti-reflective coating (ARC) on a silicon oxide pad layer, and <u>Oh</u> teaches forming an ARC on a high temperature oxidation layer that is formed over a nitride layer and a pad oxide layer. Therefore, the combination of <u>Tsai</u> and <u>Oh</u> does not teach Claim 16. Claims 17-27 are dependent on claim 16 and incorporate all of the limitations of claim 17. Therefore claims 16-27 are not obvious in light of <u>Tsai</u> in view of <u>Oh</u>.

If there are any additional charges, please charge Deposit Account No. 02-2666.

Respectfully submitted,

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